Built-In Self Test

Fulvio Corno
Maurizio Rebaudengo
Matteo Sonza Reorda

Politecnico di Torino
Dipartimento di Automatica e Informatica

Built-In Self Test

BIST is a technique aimed to:

- Avoiding the usage of expensive ATE
- Increase the fault tolerance since it add more access to the internal points
- Allow the application of at-speed test and reduce the test time.

It is mandatory to consider the BIST as a test solution when the design flow and the design area can afford it.
Disadvantages of external ATE testing

- ATE high costs
- Huge amount time spent for ATPG
- The test application through scan chain is slow
- ATEs with large memory are needed
- The circuit frequency increases more than the ATE work frequencies.

Solution

- Some ATE functionalities can be integrated within the UUT
- The UUT can be an integrated circuit, a board or the whole system
- BIST = Built-In Self Test.
BIST History

- 1978: Könemann, Mucha, Zwiehoff: BILBO
- 1981: Theus, Leutiger: first chip self-testing
- 1983: Engl, Mucha, Pfleiderer: prototype of the first self-test based microprocessor
- 1984: Kuban, Bruce: first self-testing product (Motorola MC6804P2)
Status

Nowadays the BIST is widely used for several components, such as:

- Microprocessors (Intel, Motorola, Toshiba, ecc.)
- Personal computer or Workstation, within the power-on self-test
- Electronic consumer products
- Automotive circuits (during the key-on or within the manufacturing processes).

Some first BIST products

- Motorola MC6804P2 (Microcontroller)
- Motorola MC680X0 (Microprocessor)
- Motorola MC68882 (Floating Point Processor)
- Motorola MC145532 (ADPCM Transcoder)
- Intel 80386 (Microprocessor)
- Toshiba TRON/X1 (Microprocessor)
- Apollo DN10000 (Workstation)
- etc.
Classification of the BIST strategies

Considering the phase when the test is performed it is possible to have the following BIST strategies:

- **on-line**: the test is performed during the normal functionality, it does not exist a test mode. It can be:
  - **concurrent**: the test is performed during the normal functionality of the circuit
  - **non concurrent**: the test is performed when the circuit, or one part of the circuit, is inactive
- **off-line**: the test is performed after selecting a test mode operations of the circuit.

BIST advantages

- It is oriented to solve the test problem from the radix
- It reduces the test costs
- It increments the final quality
- It reduces the TTM
- It represents the ideal solution for complex blocks dipped in other blocks
- It allows the at-speed test
- It allows both the re-use of library block either their test
- It is suitable for the wafer and core test.
**BIST disadvantages**

- It can involve upper-middle costs
- Generally demands radical changes in the plan methodologies
- It is necessary to search the more suitable solution related to the circuit architecture
- Can imply advanced consumptions regarding those typical ones of the normal operation

---

**BIST architecture**

![BIST architecture diagram]

- PI
- Test Pattern Generator
- mux
- UUT
- BIST Controller
- Output Data Evaluator
- GO/Nogo
- Normal/Test
- Reconfigure
Principal components (I)

- **Unit Under Test (UUT):** it is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. It is delimited by their Primary Input (PI) and Primary Output (PO).

- **Test Pattern Generator (TPG):** it generates the test patterns for the UUT. It is a dedicated circuit or a microprocessor. The patterns may be generated in pseudo-random or deterministically.

Principal components (II)

- **Multiplexer (mux):** it disconnects the UUT from their PI in Test Mode, it allows the TPG to apply the patterns.

- **Output Data Evaluator (ODE):** it analyses the value sequence on PO and compares it with the expected output.

- **BIST Controller:** it controls the test execution, it manages the TPG e ODE and reconfigures the UUT and the mux. It is activated by the Normal/Test signal and generates a Go/Nogo.
Principal signals

- **Normal/Test**: when it has the value “Test”, it activates a BIST session
- **Go/Nogo**: at the end of the BIST session, the “Go” value means that the UUT run correctly, “Nogo” means that at least one error has been observed
- **Reconfigure**: in some BIST architecture the UUT internal logic is reconfigured in order to improve the controllability and the observability.

Normal Mode System BIST
BIST session (I)

- Phase 1: On the signal Normal/Test it is received a command that start the test session. The command can come from an ATE, a microprocessor, or the interface Boundary Scan. It is entered in Mode Test and the BIST Controller set offs
BIST session (II)

- Phase 2: The BIST controller orders to the TPG to generate the test pattern. The patterns are applied to the UUT
- Phase 3 (parallel to the Phase 2): The BIST controller orders to the ODE to analyze the UUT outputs

Sessione BIST (III)

- Phase 4: The BIST controller analyzes the ODE’s output, compares it with the expected output for the golden circuit and update an internal flag of pass/failure. The state of this flag is sent to the external by means of the Go/Nogo signal
- Phase 5: An external circuit analyzes the Go/Nogo signal and executes the more opportune actions.
External communications

- During the phases 1 and 5 the BIST system communicates with the external world.
- Particular protocols are needed to avoid that some faults on these signals mask the faults within the circuit.
- Usually, the protocol has the signals Normal/Test and Go/Nogo.
- Particularly critical are the cases:
  - Normal/Test stuck at “Normal”
  - Go/Nogo stuck at “Go”.

Protocol example

![Diagram of BIST cell with signal transitions]

- Normal/~Test
- Go/~Nogo
- BIST Clock
- Nogo/~Go

Start

 XXXXX

End of test

clk

t

t
Note

- Go/Nogo is duplicated to avoid single points of failure (single stuck-at that invalidate the whole BIST session)
- The two signals have the opposite polarity
  - \( \text{Nogo} \sim \text{Go} = \text{not} (\text{Go} \sim \text{Nogo}) \) always
- Each wave form that differs from those specified it is considered
- Ogni forma d’onda diversa da quella specificata va considerata wrong
- The pulse of 1 clk protect against faults within the BIST controller.

Critical aspects

- The hardware for the test must be tested
- The number of I/O pins have to be minimized
- The test time have to be minimized
- The requirement to integrate the test of the BIST cell with those of the entire circuit, board or system has to be taken in consideration.